MOS NEWSFLASH

July 2003

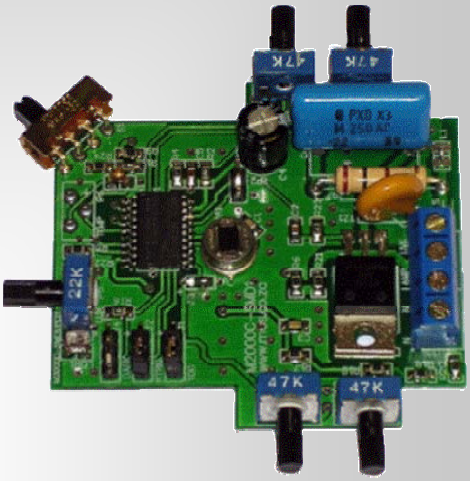
New M2000C, M2006C and M2008A PIR controllers

The latest generation of MOS PIR controllers is now available with temperature compensation. The circuit adapts the detection threshold depending on the environmental temperature. This feature drastically improves motion detection when the environmental temperature is close to the human body temperature.

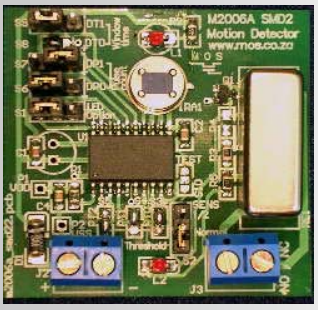
These products are equipped with a **high performance, high gain input stage**, which is directly coupled to the PIR sensor. All further signal processing is performed digitally. Drift and external component count are thereby reduced to a minimum. The combination of a second-order digital band-pass filter and the adaptive threshold detector results in unparalleled motion detection performance.

The new M2008A offers a single chip solution for 2-wire PIR Controller / Dimmer applications. Using only a few external components, a circuit can be built to replace a normal light switch with an automatic electronic version.

Ultra-low power consumption, which is only possible with custom integrated circuits, allows for significantly smaller components in the power supply circuit.



Above: The M2000C PIR evaluation module. Brightness, On-time, Sensitivity, and Fade time can be adjusted. This unit reliably detects a person at more than 12m.



Left: The M2006C evaluation module for use in alarm systems. Note the minimal component count on this single sided PCB.

MOS has been awarded the Agency for CATENA

CATENA offers a complete range of Integrated Circuit design software. The tools range from high-level VHDL design to detailed analog design. Setting up the environment for a specific foundry or technology requires minimum effort.

The software runs on Windows, Linux or Unix platforms.

Schematic Capture with SPE is easy to learn. The database is in ASCII format. Net-lists can be generated for analog and digital simulators and for Place & Route tools.

Layout development is simplified using LAYED. LAYED reads all popular layout formats (GDSII, CIF, DBX, DXF, GERBER). For those, who have to design their own custom cells, LAYED is the perfect tool.

Placement and routing of a complete chip or sections of a chip with **LAYPAR** requires very little preparation. Unlike other tools, LAYPAR works from a simple database, which is easily understood.

The LAYVER layout verification tool contains a Design Rule Checker (DRC) and a Layout Versus Schematic integrity check (LVS).

The CATENA tools enable the designer to develop complete chips from specification to final layout. These tools are available at a fraction of the cost of conventional workstation based design suites, without compromising performance or flexibility. Users can purchase modules or a complete design suite.

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