M2012B

PIR Signal Processor

General Description

The M2012B integrated circuit is designed for interfacing Passive Infra Red (PIR) sensors with micro-controllers or processors. A single wire Data Out, Clock In (DOCI) interface is provided for interfacing with a micro-controller. Multiple devices can easily be operated at the same time.

One or two PIR sensors connect directly to the PIR inputs. Pull down resistors and DC decoupling circuitry is integrated on chip. The PIR signal is converted to a 15 bit digital value.

A digital second order Butterworth low-pass filter removes unwanted higher frequency content.

The 15 bit output signal from the filter is supplied to an external microcontroller through the DOCI interface.

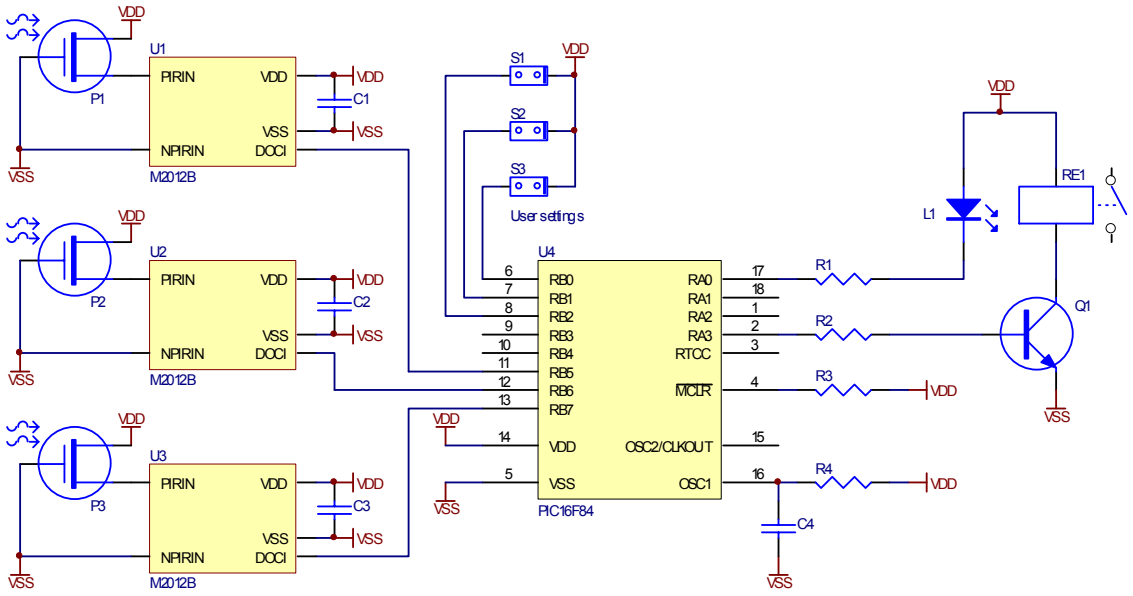
Applications

- High end PIR systems
- Multi sensor motion detectors

Features

- Digital Signal Processing (DSP)
- Differential PIR inputs
- Single wire serial interface (DOCI™)
- Operating voltage down to 3V
- Low current consumption
- High dynamic range

High-End Motion Detector Circuit



Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage	V_{DD}	-0.3	7	V	
Current into any pin		-100	100	mA	One pin at a time
Storage Temperature	T_{st}	-45	125	°C	

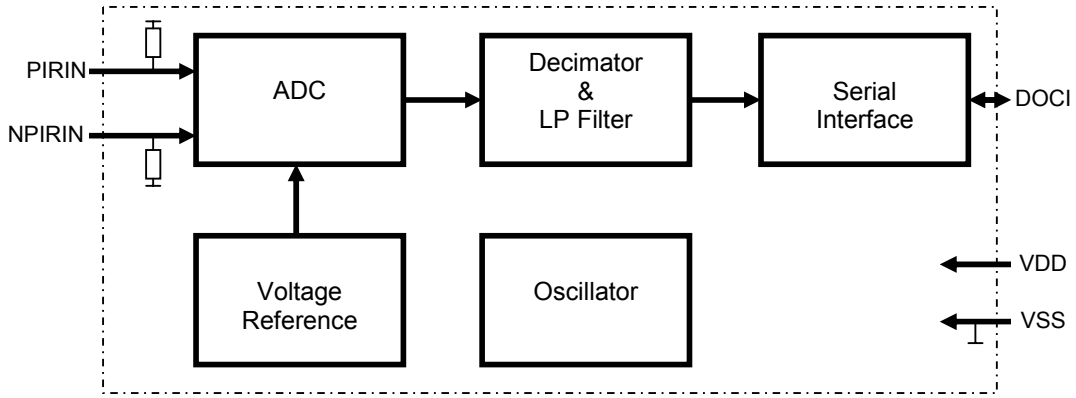
Table 1: Electrical Characteristics (Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum ratings may affect the device reliability. ESD protection: all pins will be able to withstand a discharge of a 100pF capacitor charged to 1.6kV through a 1500Ω series resistor. Test method: MIL-STD-883D method 3015).

Operating Conditions (T=25°C, VDD=5V, unless stated otherwise)

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Temperature						
Operating temperature range		-25		70	°C	
Power Supply						
Supply voltage	V_{DD}	3	5	5.5	V	
Supply current	I_{DD}			50	µA	V_{DD}=5V
DOCI Interface						
Input low voltage	V_{IL}			20	%V_{DD}	
Input high voltage	V_{IH}	80			%V_{DD}	
Pull up/down current			100		µA	Input to V_{DD} or V_{SS}
Input capacitance			5		pF	
Data setup time	t_s	2			1/F_{CLK}	
Data clock low time	t_L	200			ns	
Data clock high time	t_H	200			ns	
Data bit settling time	t_{bit}	1			µs	C_{LOAD} = 10pF
Analog Inputs PIR+,PIR-						
PIRIN input AC voltage range	V_{IAC}	-50		50	mV	PIRIN - NPIRIN
PIRIN input DC voltage range	V_{IDC}	0		V_{DD}	V	
Input impedance	R_{IN}		70		kΩ	
A/D Converter						
Resolution			14		Bits	Max Count = 2^{14}
Sensitivity			6.5		µV/count	
Temperature Coefficient	Tc	-300		300	ppm/K	
RMS noise			2.5		µV	@ 0.5 Hz
			1.5		µV	@ 1 Hz
			0.5		µV	@ 2 Hz
			0.4		µV	@ 5 Hz
Oscillator and Filter						
LPF cutoff frequency			10		Hz	
A/D Conversion time	T_{REP}		256		1/F_{CLK}	
Internal clock frequency	F_{CLK}	80	90	100	kHz	

Table 2: Operating Conditions

Detailed Description



Oscillator

The IC contains an on chip low power oscillator, with a frequency of about 90kHz. All time related signals and the cutoff frequency of the digital filter are related to the oscillator's frequency.

Input Amplifier and A/D conversion

The analog to digital converter generates a digital signal from the voltage level measured between the PIRIN and NPIRIN terminals.

Low Pass Filter

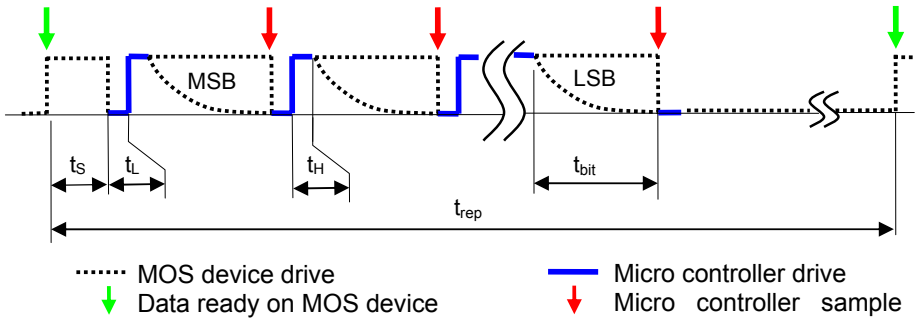
A 2nd order digital low-pass filter with decimator eliminates unwanted higher frequency components.

Serial Interface

Data is transferred from the filter to the output data latch whenever the filter has new data available and the output latch is not being read. If the micro controller reads the register faster than the update rate of the filter, the same data will be read again.

The start of a read cycle is indicated by the M2012B by pulling DOCI high.
The micro controller then generates a low to high transition on the DOCI line, before is samples the data bit. The first bit read is the MSB. This process is repeated until all 15 bits have been read. After the last bit is read, the microcontroller must force low level and subsequently release DOCI.
When a new filter value is generated, the M2012B will pull the DOCI line high and a new data byte can be read. If reading is interrupted for more than 256 system clocks with the DOCI interface at low level, the output data latch is updated with a new filter value. Reading can be interrupted, while the DOCI interface is forced high. The output latch is not updated in this condition.

DOCI Protocol



DOCI Timing

Parameter	Symbol	Min	Max	Unit	Remarks
Data register setup time	t_S	30		µs	
Data clock low time	t_L	0.2	2000	µs	
Data clock high time	t_H	0.2		µs	
Data bit settling time	t_{bit}	1		µs	

Table 3: DOCI Timing

Device Pin Out

Pin No.	Name	Description
1	TEST	Reserved test mode, connect to VSS
2	PIRIN	PIR sensor input
3	NPIRIN	PIR sensor input
4	VSS	Supply ground
5	VDDP	Positive supply
6	DOCI	Data Out Clock In, Serial interface
7	NC	Not connected
8	TCLK	Chip test clock input, can be left open or tied to VSS

Table 4: Device Pin Out

Contact Information

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Ordering Information

M2012B-SO08-150mil
M2012B-DIE